Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.An extender card comprising:

a substrate containing wiring traces for conducting signals;

first contact pads along a first edge of the substrate, the first contact pads for mating with a memory module socket on a motherboard;

a test socket, mounted to the substrate, for receiving a memory module during testing and programming;

wherein the wiring traces on the substrate include lines carrying address, data, and controls signals from the motherboard that are passed through to the test socket at pads for connecting to memory chips on the memory module;

wherein the memory chips on the memory module include a plurality of data memory chips for storing user data from the motherboard, and an error-correction code (ECC) memory chip for storing correction code generated by a code generator on the motherboard, the correction code being a pre-defined function of the user data;

wherein the wiring traces on the substrate include a plurality of first data lines and a plurality of second data

lines that carry the user data from the motherboard, and a plurality of ECC lines that carry the correction code from the motherboard;

wherein the test socket includes first contacts and second contacts that connect to the memory chips on the memory module inserted into the test socket, and ECC contacts that connect to the ECC memory chip on the memory module inserted into the test socket;

wherein the plurality of first data lines connect to the first contacts in the test socket to connect to memory chips on the memory module inserted into the test socket; and

cross-over means, on the substrate, for connecting the second data lines to the ECC contacts in the test socket and for connecting the ECC lines to the second contacts of the test socket during an ECC test mode;

wherein user data containing test patterns are written to the ECC memory chip through the cross-over means during the ECC test mode, while the correction code from the motherboard is written to one of the memory chips connected to the second contacts in the test socket.

[c2] 2.The extender card of claim 1 wherein the cross-over means comprises:

a first hardwired connection from the second data lines

to the ECC contacts of the test socket; and
a second hardwired connection from the ECC lines to the second contacts of the test socket,
whereby ECC cross-over is hardwired into the extender card.

[c3] 3.The extender card of claim 1 wherein the cross-over means comprises:
a controllable switch, having a first port receiving the second data lines, a second port receiving the ECC lines, a third port connected to the second contacts, and a fourth port connected to the ECC contacts of the test socket;
wherein the controllable switch connects the first port to the fourth port, and connects the second port to the third port, during the ECC test mode, to allow the user data that is a test pattern to be written to the ECC memory chip to test for pattern-sensitive errors in the ECC memory chip of the memory module;
wherein the controllable switch connects the first port to the third port, and connects the second port to the fourth port, during a normal mode, to allow the user data that is a test pattern to be written to the memory chips and to allow the correction code to be written to the ECC memory chip of the memory module.

[c4] 4.The extender card of claim 3 wherein the controllable switch further comprises:
a mode input, the mode input indicating the ECC test mode or the normal mode.

[c5] 5.The extender card of claim 4 wherein the mode input is connected to a mode pad of the first contact pads, the mode pad connecting to a mode signal generated by the motherboard, the mode signal being activated to indicate the ECC test mode during execution of a test program for testing the memory module inserted into the test socket.

[c6] 6.The extender card of claim 5 wherein the mode pad connects to an upper address bit generated by the motherboard, the upper address bit having a significance greater than a size of memory in the plurality of data memory chips on the memory module inserted into the test socket.

[c7] 7.The extender card of claim 1 wherein the second data lines comprise 8 data lines;
wherein the ECC lines comprise 8 lines;
whereby 8 data lines are crossed over during the ECC test mode.

[c8] 8.The extender card of claim 1 wherein the memory

chips on the memory module include a plurality N data memory chips, wherein N is a power of 2 or is double a power of 2;
wherein the ECC memory chip is a single memory chip;
wherein a total number of memory chips on the memory module is not a power of 2.

[c9] 9.The extender card of claim 1 wherein the correction code contains information sufficient for an error corrector on the motherboard to locate and correct a single bit error in the user data.

[c10] 10.A motherboard-based memory-module tester comprising:
a personal computer motherboard having a microprocessor for executing programs;
a memory controller on the personal computer motherboard for generating memory address and control signals for reading and writing user data to a memory module under test;
an error-correction code (ECC) generator on the personal computer motherboard, the ECC generator receiving user data and generating correction code;
a plurality of memory module sockets on the personal computer motherboard for receiving memory modules containing memory chips;
an extender card having lower contact pads for fitting

into one of the plurality of memory module sockets;
wherein the lower contact pads includes ECC data contacts for connecting to the ECC generator to carry the correction code, and first data contacts for carrying a first portion of the user data;
a test socket on the extender card for receiving the memory module under test, the memory module under test having a plurality of memory chips and an ECC memory chip;
wherein the test socket includes ECC data lines for connecting to data inputs of the ECC memory chip, and first data lines for connecting to data inputs of a first memory chip in the plurality of memory chips;
memory-signal wiring traces on the extender card for passing memory address and control signals through from the lower contact pads to the test socket, the memory address and control signals being generated by the personal computer motherboard to access the memory chips and the ECC memory chip on the memory module under test;
memory-data wiring traces on the extender card for passing memory data signals through from the lower contact pads to the test socket, the memory data signals being generated by the personal computer motherboard or by other memory chips in the plurality of memory chips on the memory module under test but not by the

first memory chip or by the ECC memory chip; and

cross-over wiring traces that connect the ECC data contacts to the first data lines in the test socket, and that connect the first data contacts to the ECC data lines in the test socket,

wherein the first portion of the user data is stored in the ECC memory chip;

wherein the correction code from the ECC generator on the personal computer motherboard is stored in the first memory chip in the plurality of memory chips.

[c11] 11.The motherboard-based memory-module tester of claim 10 further comprising:

a mux switch, mounted on the extender card, intercepting the cross-over wiring traces, the mux switch having a control input;

wherein the mux switch connects the ECC data contacts to the first data lines in the test socket, and connects the first data contacts to the ECC data lines in the test socket, when the control input indicates an ECC test mode;

wherein the mux switch connects the first data contacts to the first data lines in the test socket, and connects the ECC data contacts to the ECC data lines in the test socket, when the control input does not indicate the ECC test mode.

[c12] 12.The motherboard-based memory-module tester of claim 10 wherein the memory chips and the ECC memory chip are dynamic-random-access memory (DRAM).

[c13] 13.The motherboard-based memory-module tester of claim 10 wherein the correction code generated by the ECC generator and stored in the memory module under test contains information sufficient for an error corrector on the personal computer motherboard to locate and correct a single bit error in the user data.

[c14] 14.The motherboard-based memory-module tester of claim 10 wherein the memory chips on the memory module include a plurality N data memory chips, wherein N is a power of 2 or is double a power of 2;
wherein the ECC memory chip is a single memory chip;
wherein a total number of memory chips on the memory module is not a power of 2.

[c15] 15.The motherboard-based memory-module tester of claim 10 wherein the memory module under test is a registered memory module with a register and a phase-locked loop (PLL) buffer to generate clocks to the ECC memory chip and to each of the memory chips.

[c16] 16.A method for testing a memory module using a personal computer (PC) motherboard comprising:

inserting a memory module under test into a test socket, the memory module under test having memory chips and an error-correction code (ECC) memory chip;

during a first test phase,

testing the memory chips using a memory controller on the PC motherboard, by writing test pattern data to the memory chips on the memory module under test, and reading test pattern data from the memory chips on the memory module under test inserted into the test socket to test the memory chips with the test pattern data;

generating correction code for each word of the test pattern data written to the memory chips;

writing the correction code to the ECC memory chip for each word of the test pattern data;

reading the correction code from the ECC memory chip for each word of the test pattern data and comparing the correction code to a re-generated correction code generated from the test pattern data read from the memory chips to signal an error when a mis-match occurs;

during a second test phase,

crossing over data signals so that data signals to one of the memory chips is sent to the ECC memory chip wherein a portion of the test pattern data is written to the ECC memory chip; and

testing the ECC memory chip using the memory controller on the PC motherboard, by writing a portion of

the test pattern data to the ECC memory chip on the memory module under test, and reading a portion of test pattern data from the ECC memory chip on the memory module under test inserted into the test socket to test the ECC memory chip with a portion of the test pattern data.

[c17] 17.The method of claim 16 wherein the second test phase further comprises
generating correction code for each word of the test pattern data written to the memory chips;
writing the correction code to a swapped portion of the memory chips for each word of the test pattern data;
reading the correction code from the swapped portion of the memory chips for each word of the test pattern data and comparing the correction code to a re-generated correction code generated from the test pattern data read from the memory chips and from the ECC memory chip to signal an error when a mis-match occurs.

[c18] 18.The method of claim 16 wherein crossing over data signals comprises activating a mux control signal that causes a switch to connect data signals containing the portion of the test pattern data to the ECC memory chip.

[c19] 19.The method of claim 18 wherein the switch is on a cross-over extender card between the PC motherboard

and the memory module under test, or is integrated with a test socket on the PC motherboard.

[c20] 20.The method of claim 16 wherein writing to the memory chips on the memory module comprises writing to substantially all memory locations on the memory chips to test all memory locations for failures.